Fig.1

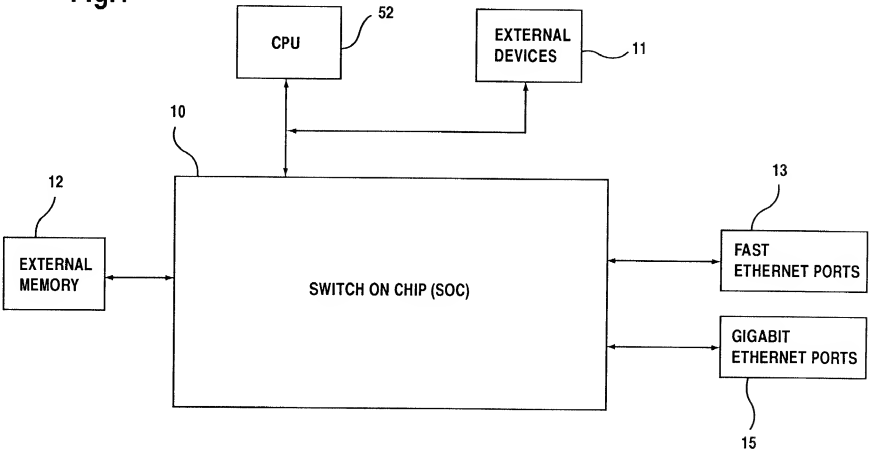

CPU
52
EXTERNAL DEVICES
11
10
12
13
EXTERNAL MEMORY
SWITCH ON CHIP (SOC)
FAST ETHERNET PORTS
GIGABIT ETHERNET PORTS
15

Fig.2

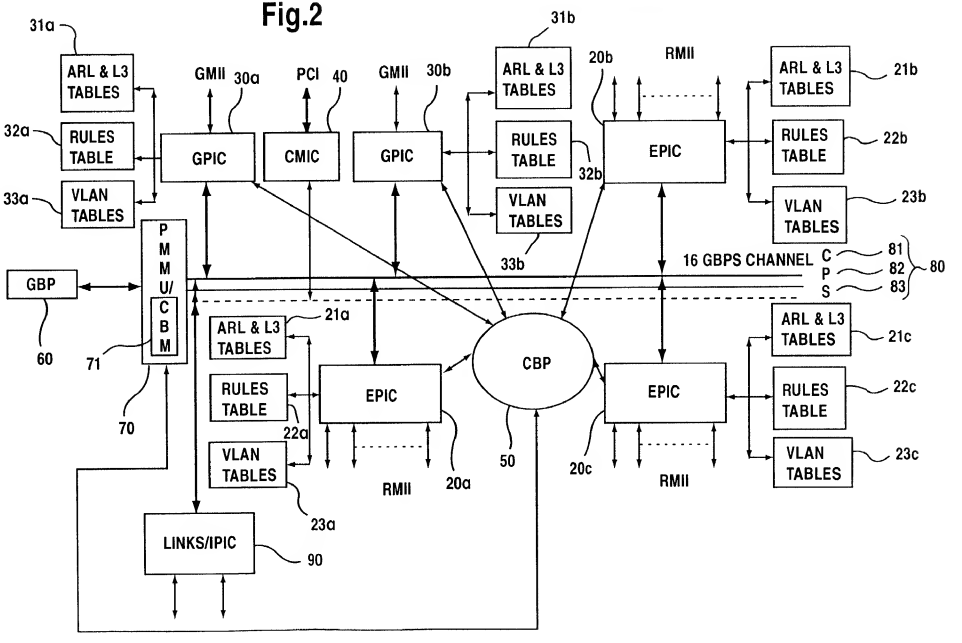


Fig.3

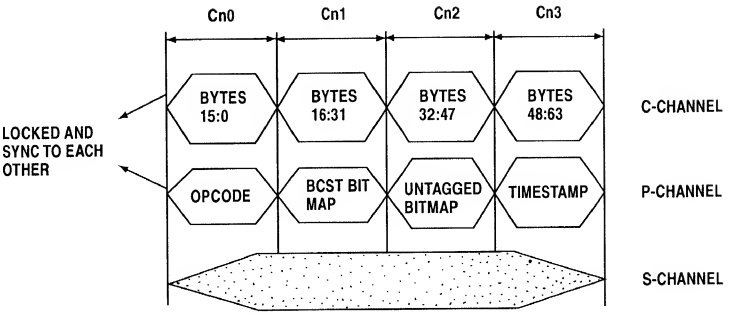


Fig.4a

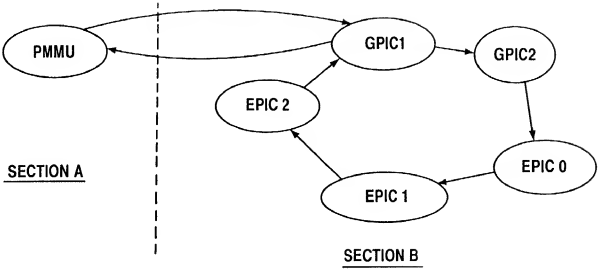

PMMU
GPIC1
GPIC2
EPIC 2
EPIC 0
EPIC 1
SECTION A
SECTION B

Fig.4b

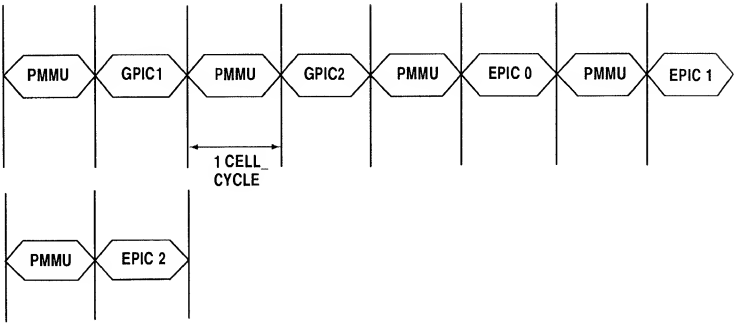

PMMU
GPIC1
PMMU
GPIC2
PMMU
EPIC 0
PMMU
EPIC 1
1 CELL CYCLE
PMMU
EPIC 2

Fig.5

PROTOCOL CHANNEL MESSAGES

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
OP CODE	IP / IPX	RESERVED	NXT CELL	SRC DEST PORT			COS	J	S / E	CRC	P / O			LEN	

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
RESERVED		BC/MC PORTBITMAP													

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
U	RES	UNTAGGED PORTBITMAP/SRC PORT NUMBER (BIT0..5)													

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
CPU OPCODES									TIME STAMP						

Fig.6

SIDE BAND CHANNEL MESSAGES

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
OPCODE			DEST PORT/ DESTINATION DEV ID			SRC PORT			DATA LEN			E	E CODE	COS	O
ADDRESS															
DATA															

Fig.7

PRIOR ART

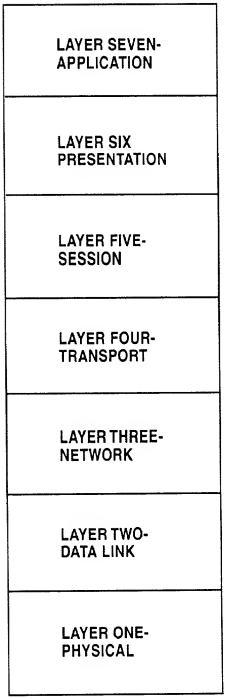


Fig.8

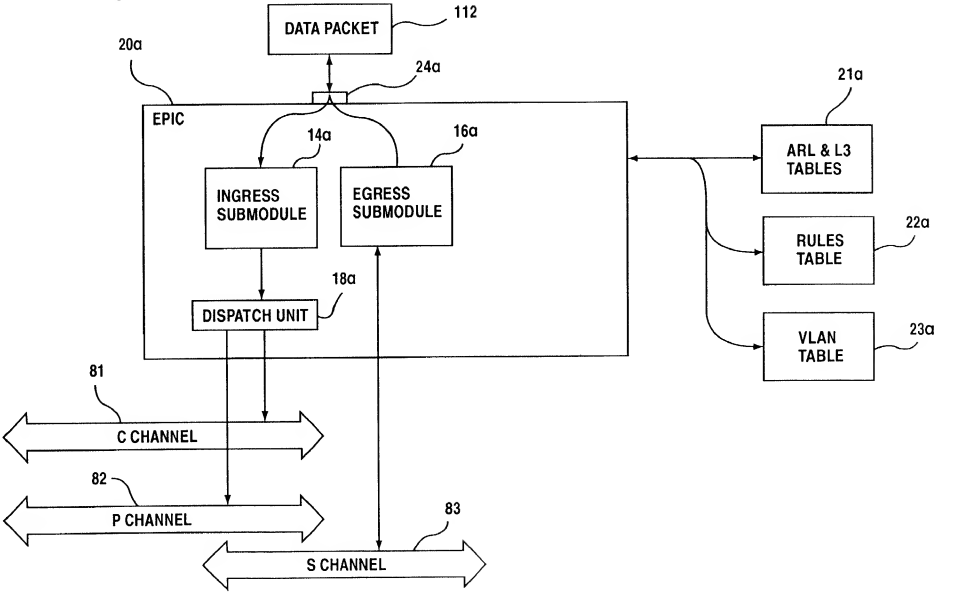

DATA PACKET
112
20a
24a
EPIC
14a
16a
INGRESS SUBMODULE
EGRESS SUBMODULE
18a
DISPATCH UNIT
21a
ARL & L3 TABLES
22a
RULES TABLE
23a
VLAN TABLE
81
C CHANNEL
82
P CHANNEL
83
S CHANNEL

Fig.9

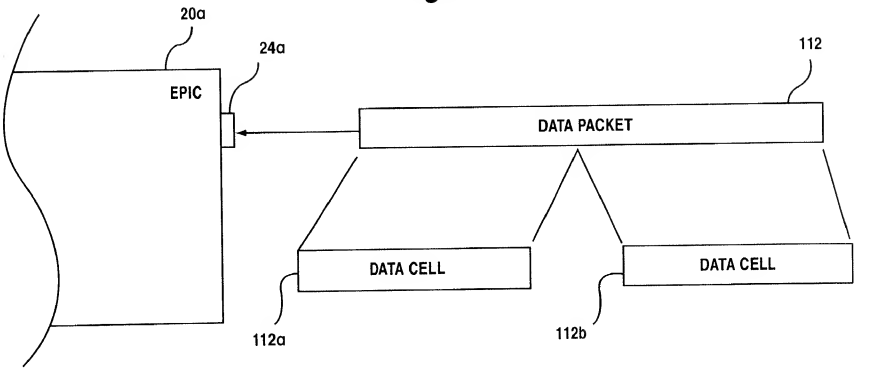


Fig.10

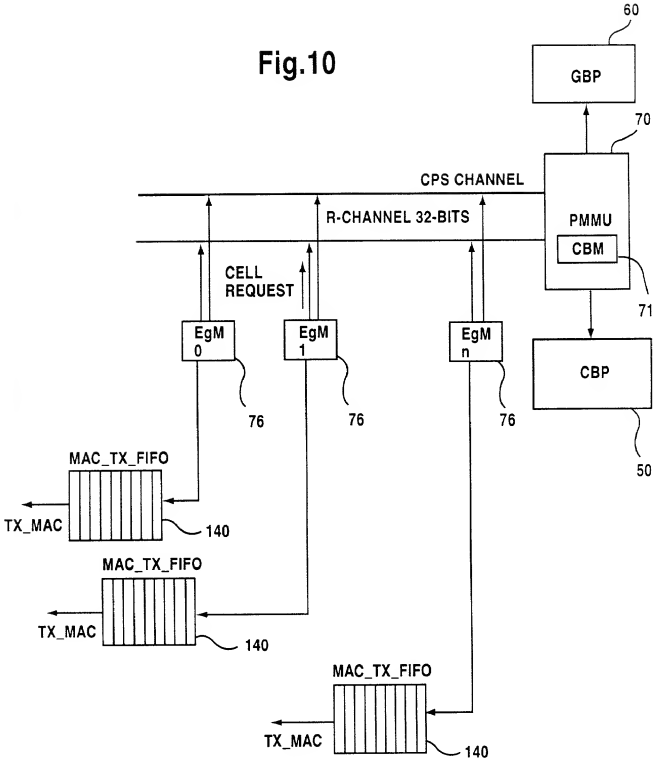

60
GBP
70
CPS CHANNEL
R-CHANNEL 32-BITS
PMMU
CBM
71
CELL
REQUEST
EgM
0
EgM
1
EgM
n
CBP
76
76
76
50
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140

Fig.11

LINE 0 →	FC | LC | BC/MC | CPY_CNT(5b) | CELL_LENGTH (7b) | CRC (2b) | NC_HEADER (16b) | SRC COUNT(6) | IPX | IP | TIME_STAMP (14b) | 0 BITS(2b) | P | NEXT CELL LEN (2b) | CPU OPCODE (4b) | CELL_DATA (0-9B)
LINE 1 →	CELL_DATA (10-27) BYTES
LINE 2 →	CELL_DATA (28-45) BYTES
LINE 3 →	CELL_DATA (46-63) BYTES

Fig.12

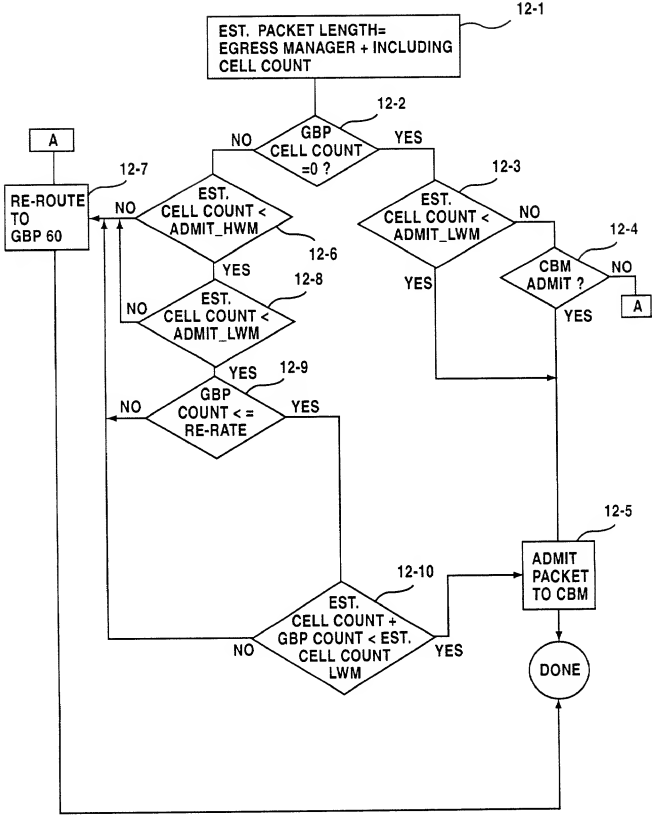

12-1
EST. PACKET LENGTH= EGRESS MANAGER + INCLUDING CELL COUNT
12-2
GBP CELL COUNT =0 ?
NO
YES
A
12-7
RE-ROUTE TO GBP 60
EST. CELL COUNT < ADMIT_HWM
NO
12-6
YES
12-3
EST. CELL COUNT < ADMIT_LWM
NO
YES
12-4
CBM ADMIT ?
NO
A
YES
12-8
EST. CELL COUNT < ADMIT_LWM
NO
YES
12-9
GBP COUNT < = RE-RATE
NO
YES
12-5
ADMIT PACKET TO CBM
12-10
EST. CELL COUNT + GBP COUNT < EST. CELL COUNT LWM
NO
YES
DONE

Fig.13

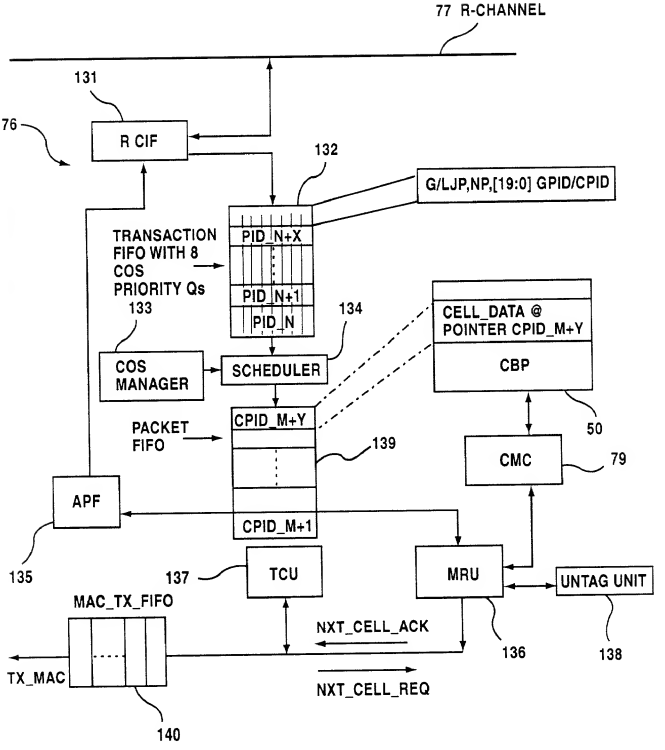

77 R-CHANNEL
131
76
R CIF
132
G/LJP,NP,[19:0] GPID/CPID
TRANSACTION FIFO WITH 8 COS PRIORITY Qs
PID_N+X
PID_N+1
PID_N
133
134
CELL_DATA @ POINTER CPID_M+Y
CBP
COS MANAGER
SCHEDULER
50
PACKET FIFO
CPID_M+Y
139
CMC
79
APF
CPID_M+1
135
137
TCU
MRU
UNTAG UNIT
MAC_TX_FIFO
NXT_CELL_ACK
136
138
TX_MAC
NXT_CELL_REQ
140

Fig.14

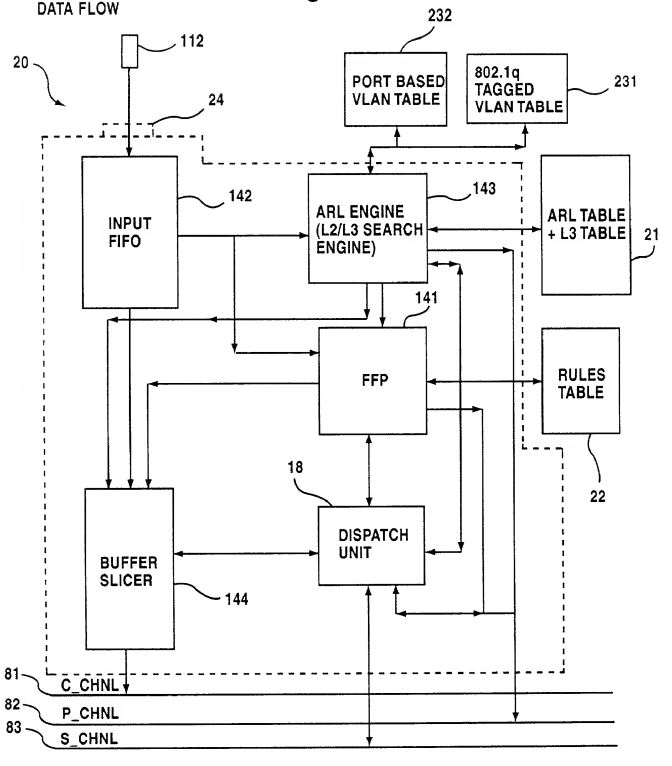

DATA FLOW
20
112
24
232
PORT BASED VLAN TABLE
802.1q TAGGED VLAN TABLE
231
INPUT FIFO
142
ARL ENGINE (L2/L3 SEARCH ENGINE)
143
ARL TABLE + L3 TABLE
21
141
FFP
RULES TABLE
22
18
DISPATCH UNIT
BUFFER SLICER
144
81
C_CHNL
82
P_CHNL
83
S_CHNL

Fig.15

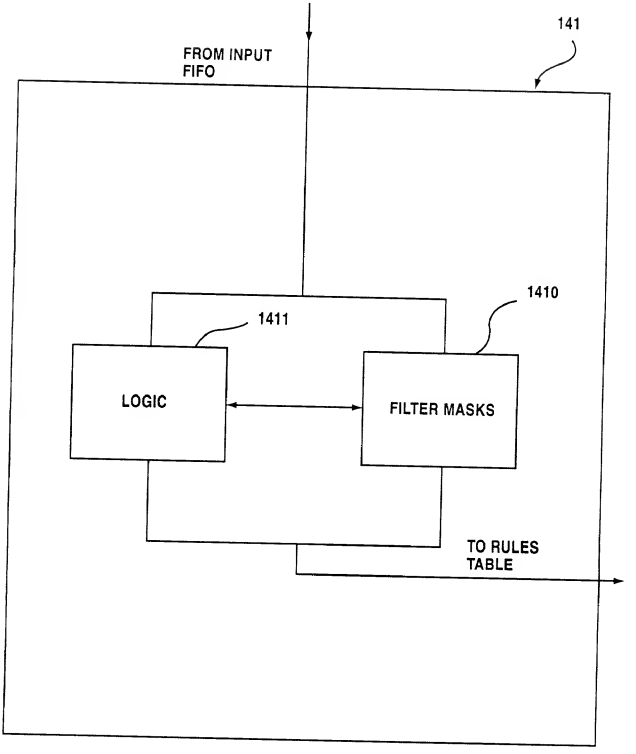

141
FROM INPUT FIFO
1410
1411
LOGIC
FILTER MASKS
TO RULES TABLE

Fig.16

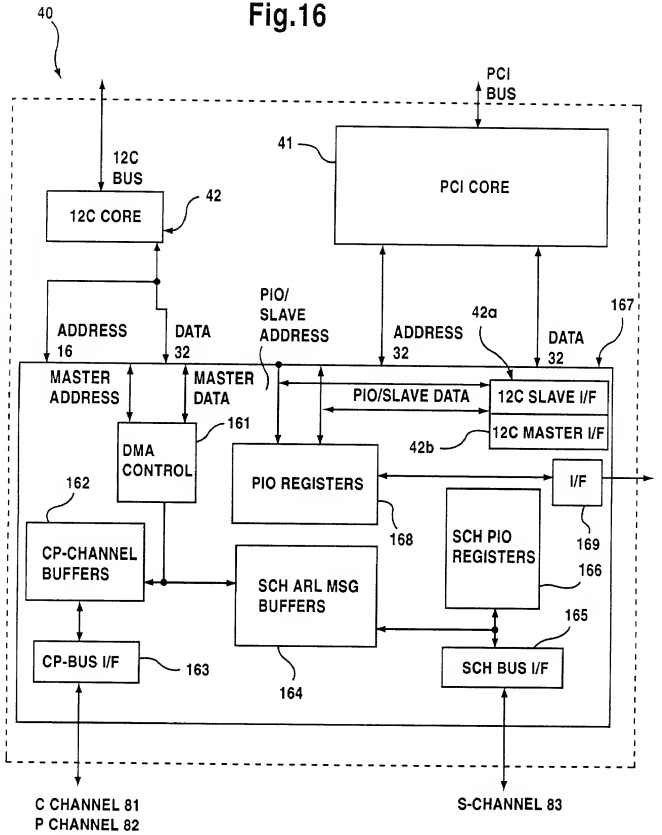

40
PCI BUS
41
PCI CORE
12C BUS
12C CORE
42
ADDRESS 16
DATA 32
PIO/ SLAVE ADDRESS
ADDRESS 32
42a
DATA 32
167
MASTER ADDRESS
MASTER DATA
PIO/SLAVE DATA
12C SLAVE I/F
12C MASTER I/F
42b
DMA CONTROL
161
PIO REGISTERS
I/F
162
168
169
CP-CHANNEL BUFFERS
SCH ARL MSG BUFFERS
SCH PIO REGISTERS
166
165
CP-BUS I/F
163
164
SCH BUS I/F
C CHANNEL 81
P CHANNEL 82
S-CHANNEL 83

Fig.17

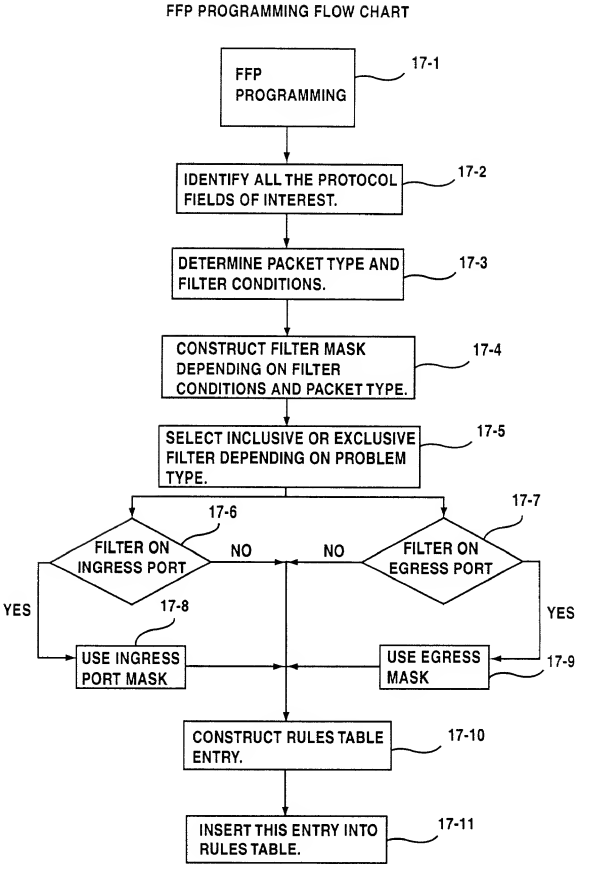

FFP PROGRAMMING FLOW CHART
FFP PROGRAMMING
17-1
IDENTIFY ALL THE PROTOCOL FIELDS OF INTEREST.
17-2
DETERMINE PACKET TYPE AND FILTER CONDITIONS.
17-3
CONSTRUCT FILTER MASK DEPENDING ON FILTER CONDITIONS AND PACKET TYPE.
17-4
SELECT INCLUSIVE OR EXCLUSIVE FILTER DEPENDING ON PROBLEM TYPE.
17-5
17-6
FILTER ON INGRESS PORT
NO
NO
17-7
FILTER ON EGRESS PORT
YES
17-8
USE INGRESS PORT MASK
USE EGRESS MASK
17-9
YES
CONSTRUCT RULES TABLE ENTRY.
17-10
INSERT THIS ENTRY INTO RULES TABLE.
17-11

Fig.18

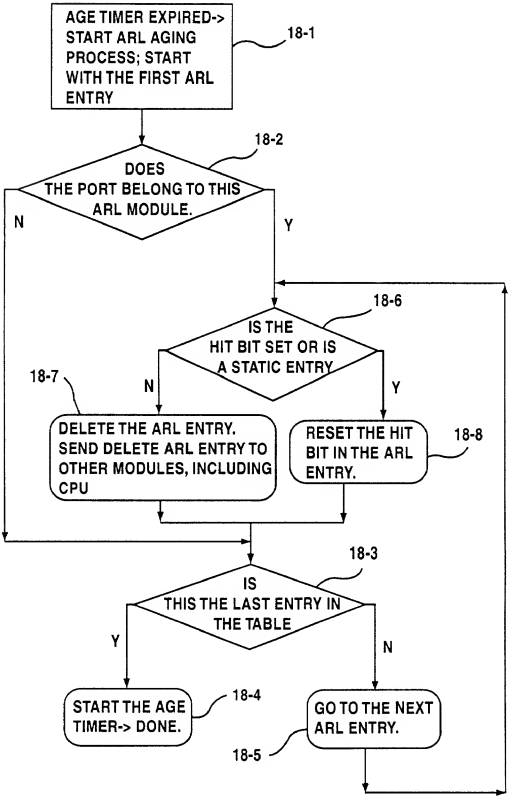

AGE TIMER EXPIRED-> START ARL AGING PROCESS; START WITH THE FIRST ARL ENTRY
18-1
18-2
DOES THE PORT BELONG TO THIS ARL MODULE.
N
Y
18-6
IS THE HIT BIT SET OR IS A STATIC ENTRY
18-7
N
Y
DELETE THE ARL ENTRY. SEND DELETE ARL ENTRY TO OTHER MODULES, INCLUDING CPU
RESET THE HIT BIT IN THE ARL ENTRY.
18-8
18-3
IS THIS THE LAST ENTRY IN THE TABLE
Y
N
START THE AGE TIMER-> DONE.
18-4
GO TO THE NEXT ARL ENTRY.
18-5

Fig.19

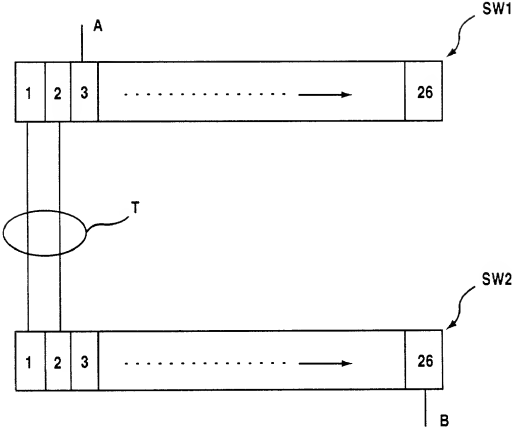


Fig.20

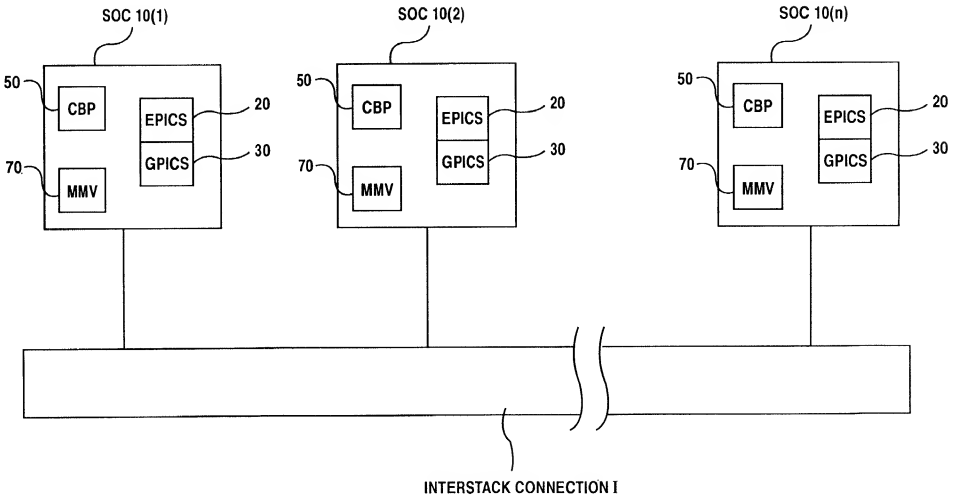

SOC 10(1)
SOC 10(2)
SOC 10(n)
50
CBP
EPICS
20
GPICS
30
70
MMV
INTERSTACK CONNECTION I

Fig.21

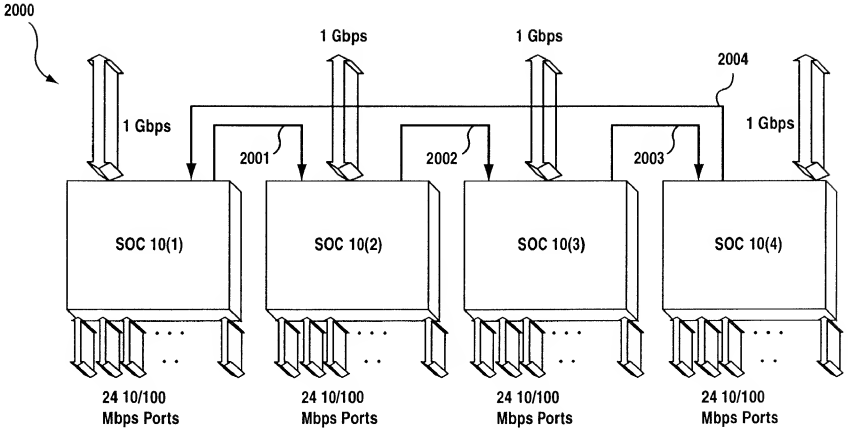


Fig.22

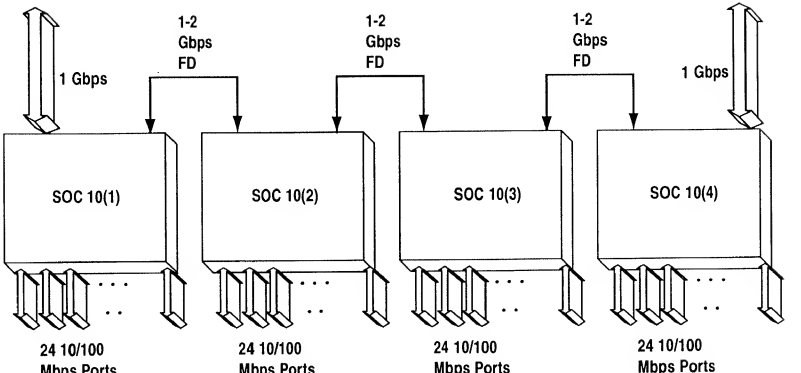


Fig.23

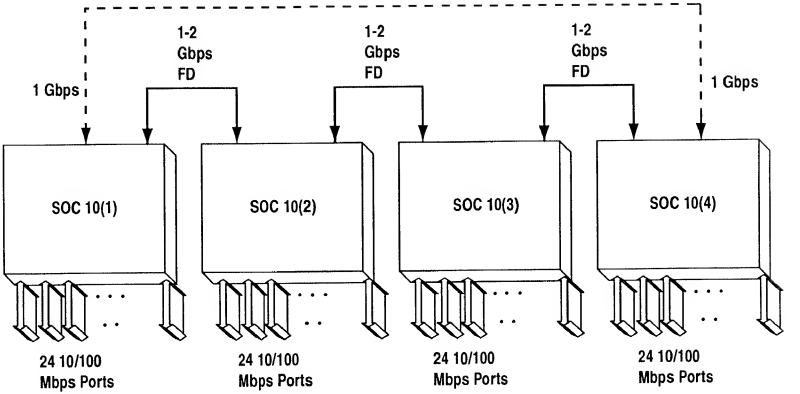

1 Gbps
1-2 Gbps FD
1-2 Gbps FD
1-2 Gbps FD
1 Gbps
SOC 10(1)
SOC 10(2)
SOC 10(3)
SOC 10(4)
24 10/100 Mbps Ports
24 10/100 Mbps Ports
24 10/100 Mbps Ports
24 10/100 Mbps Ports

Fig.24A

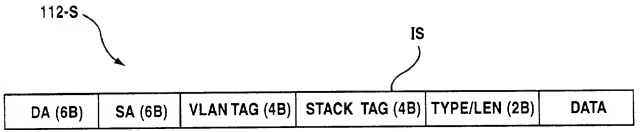


Fig.24B

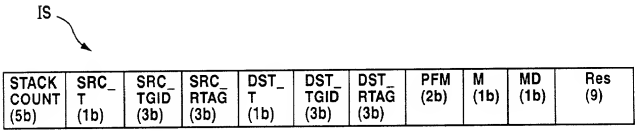


Fig.25

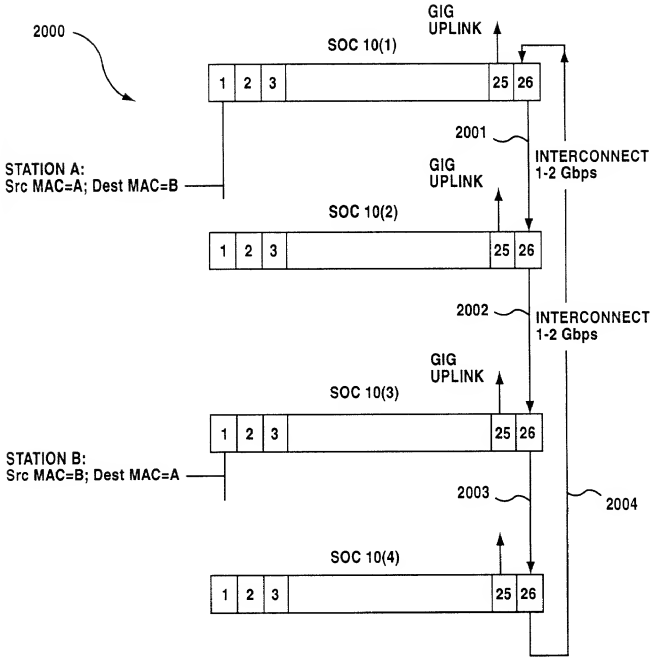

2000
GIG
UPLINK
SOC 10(1)
1
2
3
25
26
2001
INTERCONNECT
1-2 Gbps
STATION A:
Src MAC=A; Dest MAC=B
GIG
UPLINK
SOC 10(2)
2002
INTERCONNECT
1-2 Gbps
GIG
UPLINK
SOC 10(3)
STATION B:
Src MAC=B; Dest MAC=A
2003
2004
SOC 10(4)

Fig.26

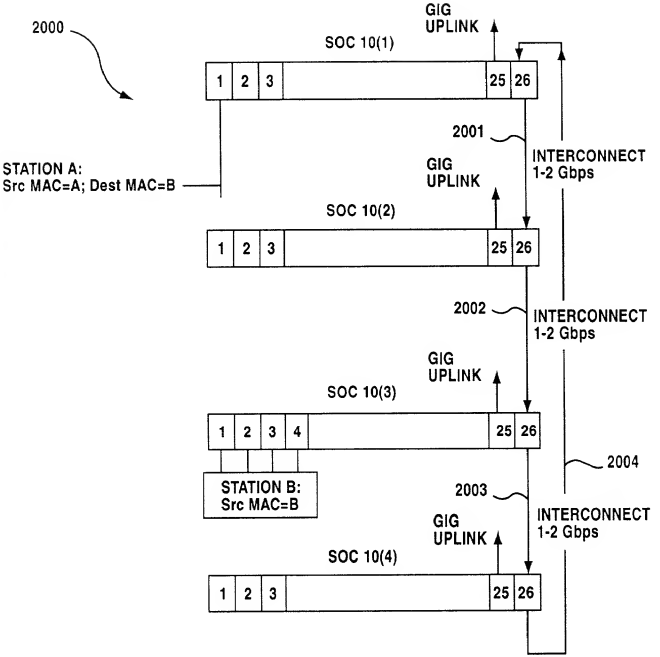

2000
GIG UPLINK
SOC 10(1)
1 2 3
25 26
2001
INTERCONNECT 1-2 Gbps
STATION A: Src MAC=A; Dest MAC=B
GIG UPLINK
SOC 10(2)
1 2 3
25 26
2002
INTERCONNECT 1-2 Gbps
GIG UPLINK
SOC 10(3)
1 2 3 4
25 26
2004
STATION B: Src MAC=B
2003
GIG UPLINK
INTERCONNECT 1-2 Gbps
SOC 10(4)
1 2 3
25 26

Fig.27A

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
1	A	1	0	X	X
26	B	1	1	2	2

Fig.27B

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	0	X	X
26	B	1	1	2	2

Fig.27C

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	0	X	X
1	B	1	1	2	2

Fig.27D

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	0	X	X
26	B	1	1	2	2

Fig.28

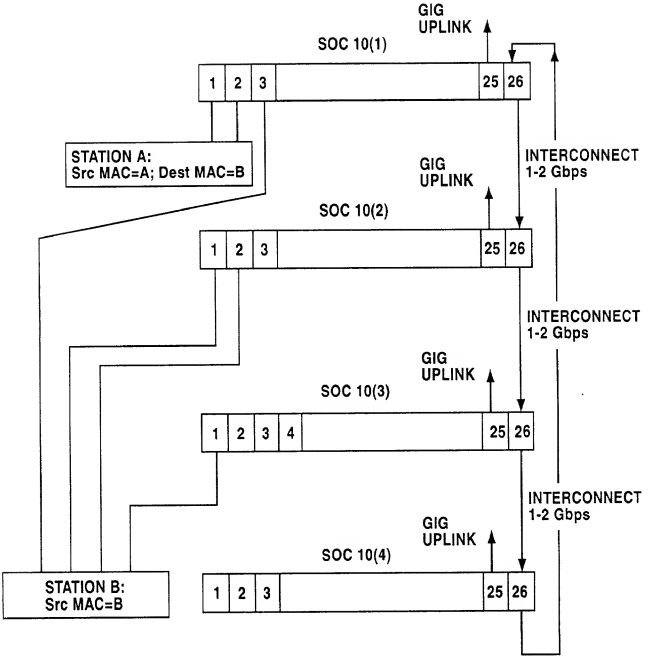

GIG
UPLINK
SOC 10(1)
1
2
3
25
26
STATION A:
Src MAC=A; Dest MAC=B
GIG
UPLINK
INTERCONNECT
1-2 Gbps
SOC 10(2)
1
2
3
25
26
INTERCONNECT
1-2 Gbps
GIG
UPLINK
SOC 10(3)
1
2
3
4
25
26
INTERCONNECT
1-2 Gbps
GIG
UPLINK
SOC 10(4)
STATION B:
Src MAC=B
1
2
3
25
26

Fig.29

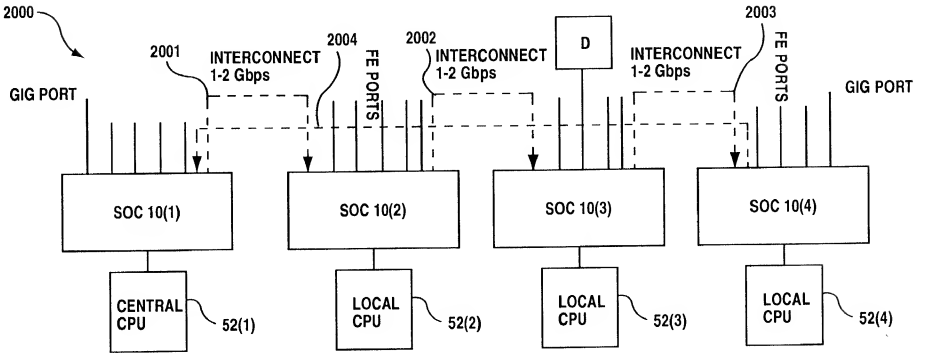

2000
2001
INTERCONNECT
1-2 Gbps
2004
FE PORTS
2002
INTERCONNECT
1-2 Gbps
D
INTERCONNECT
1-2 Gbps
2003
FE PORTS
GIG PORT
GIG PORT
SOC 10(1)
SOC 10(2)
SOC 10(3)
SOC 10(4)
CENTRAL CPU
52(1)
LOCAL CPU
52(2)
LOCAL CPU
52(3)
LOCAL CPU
52(4)

Fig.30

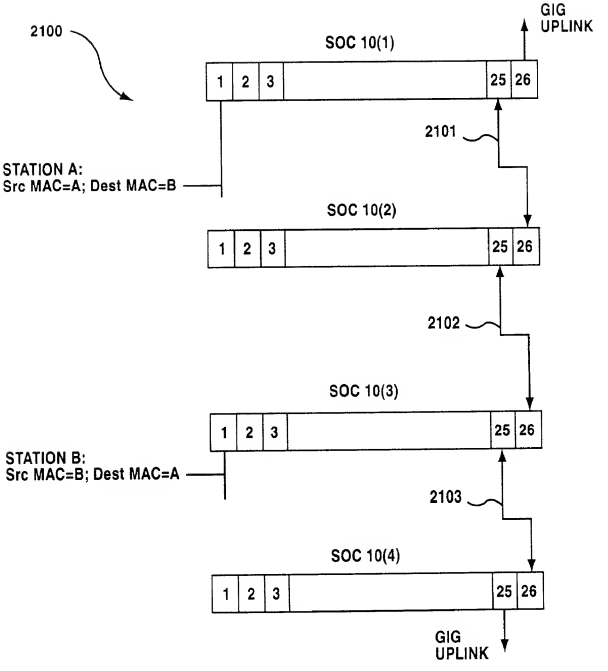

2100
GIG UPLINK
SOC 10(1)
1 2 3
25 26
2101
STATION A:
Src MAC=A; Dest MAC=B
SOC 10(2)
1 2 3
25 26
2102
SOC 10(3)
1 2 3
25 26
STATION B:
Src MAC=B; Dest MAC=A
2103
SOC 10(4)
1 2 3
25 26
GIG UPLINK

Fig.31

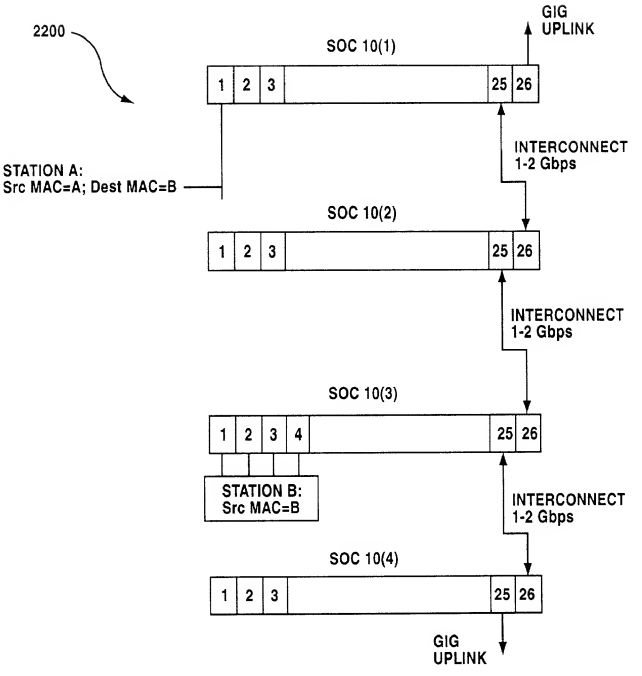

2200
GIG
UPLINK
SOC 10(1)
1
2
3
25
26
INTERCONNECT
1-2 Gbps
STATION A:
Src MAC=A; Dest MAC=B
SOC 10(2)
1
2
3
25
26
INTERCONNECT
1-2 Gbps
SOC 10(3)
1
2
3
4
25
26
STATION B:
Src MAC=B
INTERCONNECT
1-2 Gbps
SOC 10(4)
1
2
3
25
26
GIG
UPLINK

Fig.32A

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
1	A	1	0	X	X
25	B	1	1	2	2

Fig.32B

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	0	X	X
25	B	1	1	2	2

Fig.32C

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	0	X	X
1	B	1	1	2	2

Fig.32D

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	0	X	X

Fig.33

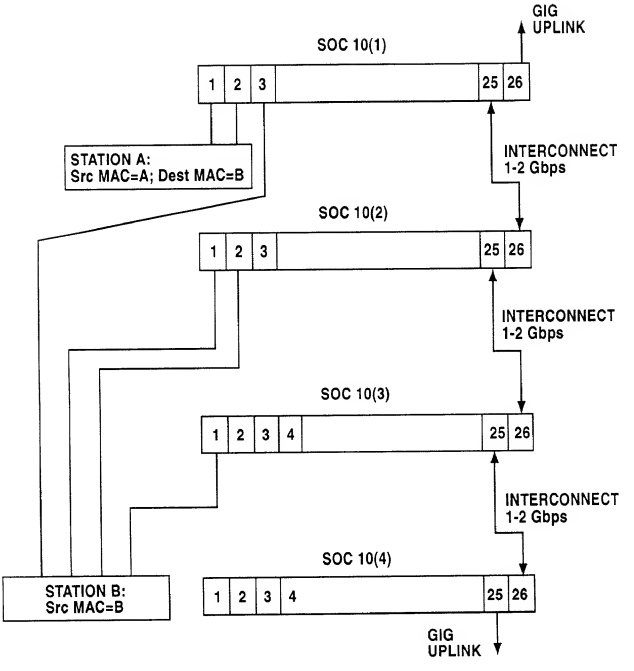

GIG
UPLINK
SOC 10(1)
1
2
3
25
26
STATION A:
Src MAC=A; Dest MAC=B
INTERCONNECT
1-2 Gbps
SOC 10(2)
1
2
3
25
26
INTERCONNECT
1-2 Gbps
SOC 10(3)
1
2
3
4
25
26
INTERCONNECT
1-2 Gbps
SOC 10(4)
STATION B:
Src MAC=B
1
2
3
4
25
26
GIG
UPLINK

Fig.34A

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
1	A	1	1	1	1
25	B	1	1	2	2

Fig.34B

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	1	1	1
25	B	1	1	2	2

Fig.34C

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	1	1	1
1	B	1	1	2	2

Fig.34D

PORT NUMBER	MAC ADDRESS	VLAN ID	T	TGID	RTAG
26	A	1	1	1	1

Fig.35

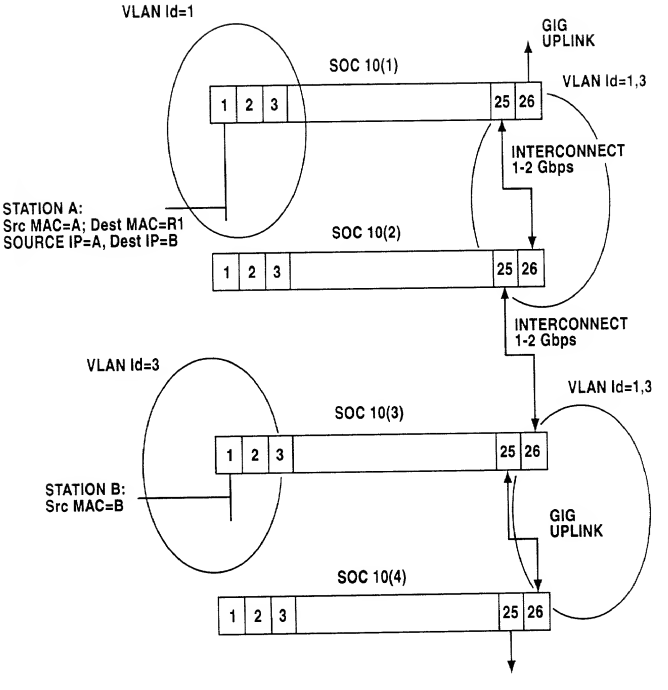

VLAN Id=1
GIG
UPLINK
SOC 10(1)
VLAN Id=1,3
1 2 3
25 26
INTERCONNECT
1-2 Gbps
STATION A:
Src MAC=A; Dest MAC=R1
SOURCE IP=A, Dest IP=B
SOC 10(2)
1 2 3
25 26
INTERCONNECT
1-2 Gbps
VLAN Id=3
VLAN Id=1,3
SOC 10(3)
1 2 3
25 26
STATION B:
Src MAC=B
GIG
UPLINK
SOC 10(4)
1 2 3
25 26

Fig.36

TRUNK GROUP TABLE FOR SW1:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG SIZE
2	25	25	25	25	X	X	X	X	4

TRUNK GROUP TABLE FOR SW2:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG SIZE
2	25	25	25	25	X	X	X	X	4

TRUNK GROUP TABLE FOR SW3:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG SIZE
2	1	2	3	4	X	X	X	X	4

TRUNK GROUP TABLE FOR SW4:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG SIZE
2	26	26	26	26	X	X	X	X	4

Fig.37

TRUNK GROUP TABLE FOR SW1:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG SIZE
1	1	2	X	X	X	X	X	X	2
2	25	25	25	3	X	X	X	X	4

TRUNK GROUP TABLE FOR SW2:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG SIZE
1	26	26	X	X	X	X	X	X	2
2	25	1	2	26	X	X	X	X	4

TRUNK GROUP TABLE FOR SW3:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG SIZE
1	26	26	X	X	X	X	X	X	2
2	1	26	26	26	X	X	X	X	4

TRUNK GROUP TABLE FOR SW4:

TGID	TP0	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TG SIZE
1	26	26	X	X	X	X	X	X	2
2	26	26	26	26	X	X	X	X	4

Fig.38

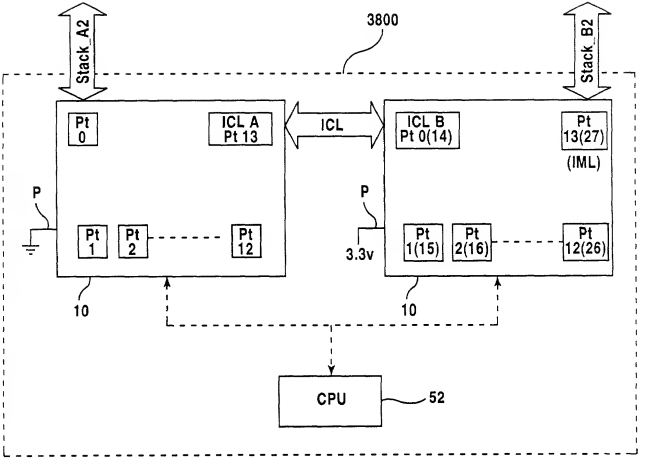
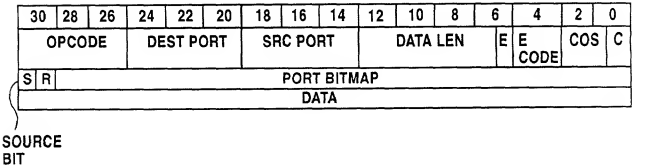
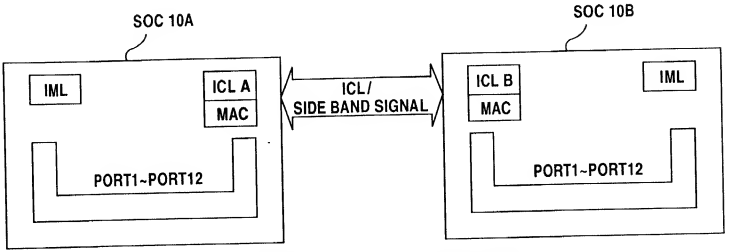

3800
Stack_A2
Stack_B2
Pt 0
ICL A Pt 13
ICL
ICL B Pt 0(14)
Pt 13(27)
(IML)
P
P
Pt 1
Pt 2
Pt 12
3.3v
Pt 1(15)
Pt 2(16)
Pt 12(26)
10
10
CPU
52

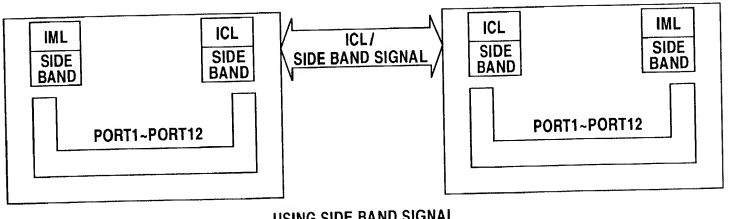
Fig.39


30 28 26 24 22 20 18 16 14 12 10 8 6 4 2 0
OPCODE
DEST PORT
SRC PORT
DATA LEN
E
E CODE
COS
C
S
R
PORT BITMAP
DATA
SOURCE BIT



USING MAC CONTROL FRAME SCHEME

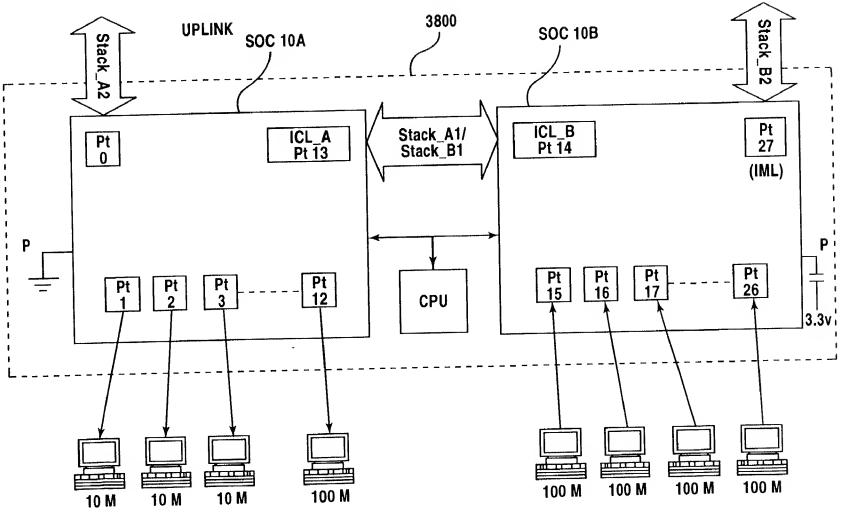
Fig.40



USING SIDE BAND SIGNAL

Fig.41

Fig.42


Stack_A2
UPLINK
SOC 10A
3800
SOC 10B
Stack_B2
Pt 0
ICL_A Pt 13
Stack_A1/ Stack_B1
ICL_B Pt 14
Pt 27
(IML)
P
P
Pt 1
Pt 2
Pt 3
Pt 12
CPU
Pt 15
Pt 16
Pt 17
Pt 26
3.3v
10 M
10 M
10 M
100 M
100 M
100 M
100 M
100 M

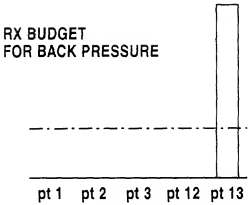


Fig.43A

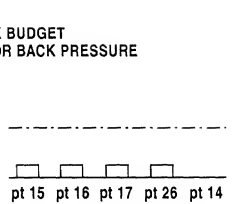


Fig.43B

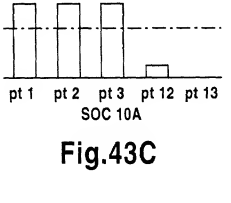


Fig.43C

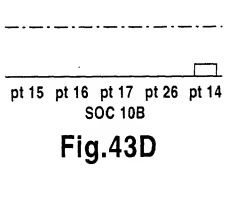


Fig.43D

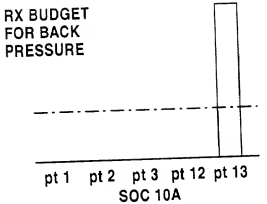


Fig.44A

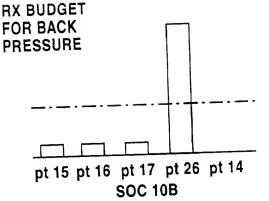


Fig.44B

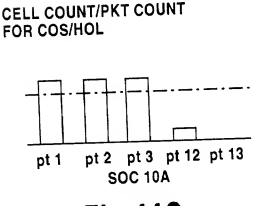


Fig.44C

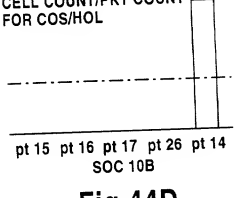


Fig.44D

Fig.45

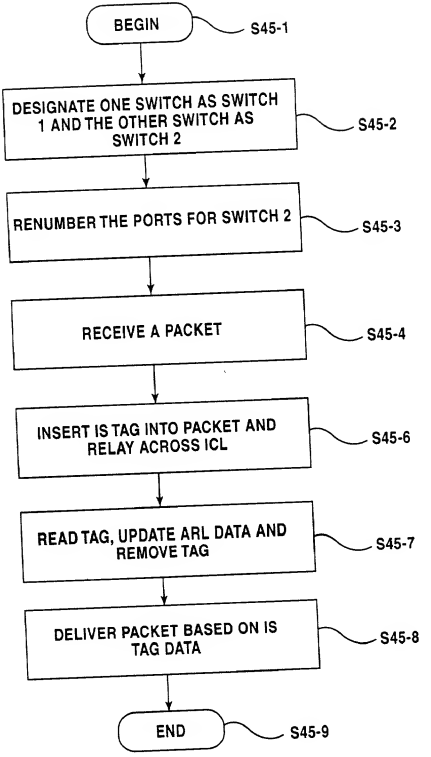

BEGIN
S45-1
DESIGNATE ONE SWITCH AS SWITCH 1 AND THE OTHER SWITCH AS SWITCH 2
S45-2
RENUMBER THE PORTS FOR SWITCH 2
S45-3
RECEIVE A PACKET
S45-4
INSERT IS TAG INTO PACKET AND RELAY ACROSS ICL
S45-6
READ TAG, UPDATE ARL DATA AND REMOVE TAG
S45-7
DELIVER PACKET BASED ON IS TAG DATA
S45-8
END
S45-9

Fig.46

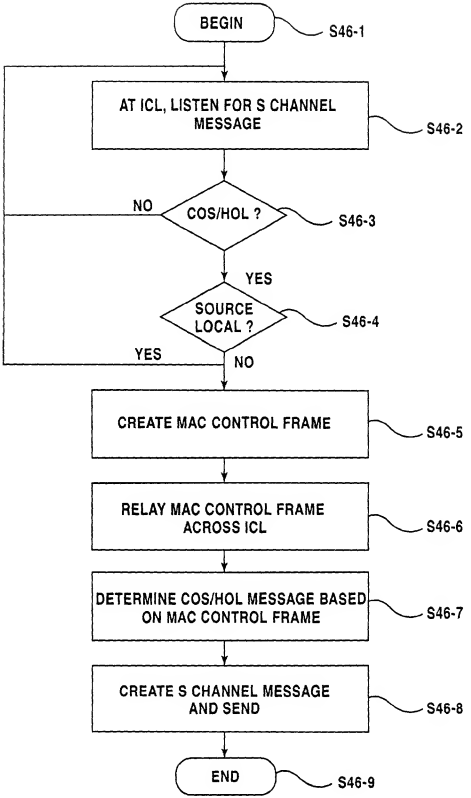
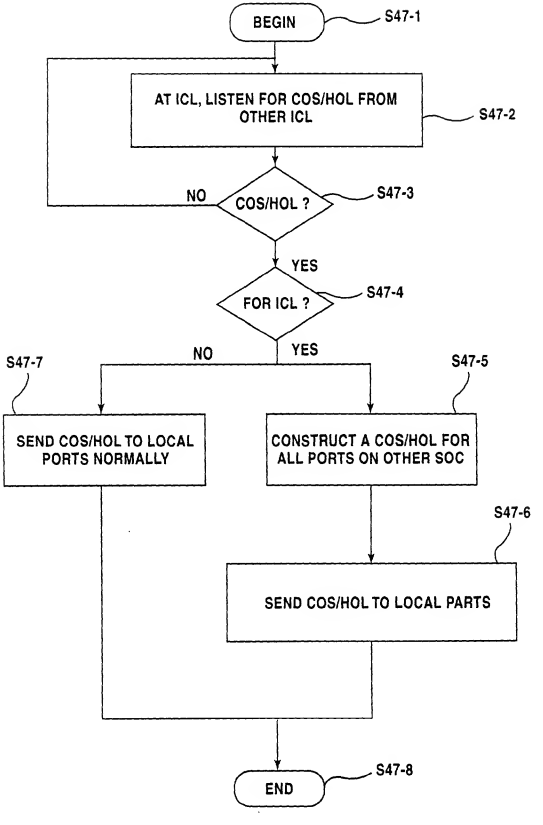

BEGIN
S46-1
AT ICL, LISTEN FOR S CHANNEL MESSAGE
S46-2
NO
COS/HOL ?
S46-3
YES
SOURCE LOCAL ?
S46-4
YES
NO
CREATE MAC CONTROL FRAME
S46-5
RELAY MAC CONTROL FRAME ACROSS ICL
S46-6
DETERMINE COS/HOL MESSAGE BASED ON MAC CONTROL FRAME
S46-7
CREATE S CHANNEL MESSAGE AND SEND
S46-8
END
S46-9

Fig.47


BEGIN
S47-1
AT ICL, LISTEN FOR COS/HOL FROM OTHER ICL
S47-2
NO
COS/HOL ?
S47-3
YES
FOR ICL ?
S47-4
NO
YES
S47-7
S47-5
SEND COS/HOL TO LOCAL PORTS NORMALLY
CONSTRUCT A COS/HOL FOR ALL PORTS ON OTHER SOC
S47-6
SEND COS/HOL TO LOCAL PARTS
END
S47-8